User's Manual

The iPORT™ PT1000-VB
In-Camera IP Engine

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1.0 Introduction

1.1 The Scope of this User's Manual

This User's Manual describes how to access and use the features in Pleora's iPORT PT1000-VB In-Camera IP Engine.

1.2 Related Documents

The iPORT PT1000-VB IP Engine is one member of Pleora's growing family of iPORT IP Engines. For information about other available engine models, visit www.pleora.com. All the engines share one set of core features, described in a document entitled "User's Manual, Shared Features of iPORT IP Engines."

iPORT PT1000-VB IP Engine is an element of the iPORT Connectivity Solution. As such, it is shipped with two PC applications: the iPORT IP Device Driver; and the iPORT Software Development Kit (SDK – available in C++ or Visual Basic). These software applications have their own documentation.

The iPORT Connectivity Solution also includes the iPORT High Memory Manager, which is described in the iPORT IP Device Drivers manual. As an option, the solution can also include iPORT Hydra™ PC Communications Software, described in the SDK C++ manual.

For PT1000-VB customers seeking to achieve EMI certification for their products, Pleora has prepared a separate document entitled "iPORT PT1000-VB In-Camera IP Engine, Design Recommendations for FCC/CE Certification."

In summary, this User's Manual complements, and should be used in conjunction with, up to five other documents:

- User's Manual, Shared Features of iPORT IP Engines;
- User's Manual, iPORT IP Device Drivers;
- Reference Manual, The iPORT C++ Software Development Kit;
- Reference Manual, The iPORT Visual Basic Software Development Kit; and
- iPORT PT1000-VB In-Camera IP Engine: Design Recommendations for FCC/CE Certification

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2.0 Overview of the iPORT PT1000-VB

2.1 Highlights

Pleora's iPORT PT1000-VB In-Camera IP Engine is a fast, affordable, and simple way to integrate high-performance GigE connectivity into industrial cameras. The board is ideal for GigE-enabling cameras targeted at demanding vision applications in product inspection, security/surveillance, traffic monitoring, and post and parcel sorting.

The PT1000-VB is also ready to comply with the AIA's (Automated Imaging Association) GigE Vision™ standard.

The engine is optimized for in-camera use, with a small, square footprint, low power consumption, and vertical mounts for power, GPIO, and GigE. Straightforward interfaces to parallel data, clocks, line, and frame signals allow most cameras, including Camera Link® models, to support GigE with a simple change-out to their back-end electronics.

Purpose-built hardware is used instead of an embedded processor. This allows the engine to acquire, packetize, and drive camera data onto GigE links or LANs with ultra-efficient, clock-cycle accuracy.

The PT1000-VB processes image data continuously at GigE's full 1-Gb/s line rate, while delivering low, predictable latencies. A unique IP transfer protocol guarantees the delivery of every packet, ensuring best-in-class performance.

The high throughput of the board supports real-time operation with most image sensors, including performance-oriented CCD sensors with fast frame rates.

At all throughput rates, the PT1000-VB consumes less than 2.25 W of power, making it an easy fit for small-body cameras with strict power budgets.

The PT1000-VB also handles control signals from the PC and other system elements. These signals are routed through a PLC (programmable logic controller) that allows users to precisely measure and control the operation of conveyors, encoders, cameras, and other components – either independently from or in conjunction with the host PC on the network.

As one element of Pleora's end-to-end iPORT Connectivity Solution, the iPORT PT1000-VB is shipped with two powerful PC applications. The iPORT IP Device Driver streams data to PC memory using minimal CPU capacity. Users can choose from two versions: the iPORT High-Performance IP Device Driver or the iPORT Universal IP Filter Driver. The iPORT SDK gives users the building blocks needed to quickly and easily enable third-party or custom video applications. For more information about the iPORT Connectivity Solution, see the "User's Manual, Shared Features of iPORT IP Engines."

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2.2 Models

The first available model in Pleora's family of in-camera IP engines is the iPORT PT1000-VB-CL. This model is designed specifically for integration into cameras using the Camera Link protocol. It is equipped with an FPGA load that accommodates the Camera Link interface and, in keeping with the protocol, encapsulates a serial communications channel over GigE. This allows users to update camera configuration registers from a host PC.

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2.3 Characteristics and Features

Table 1 lists key characteristics and features of the iPORT PT1000-VB-CL.

Hardware	
Available as OEM	Yes
Onboard Memory	16 MB
Inputs/Outputs	
TTL Inputs	4
TTL Outputs	3
Camera Control Outputs	4 x LVTTL
Programmable Logic Control	
Pulse Generators (timers)	4
Rescaler (16-bit)	1
Delayers	1
General Purpose Counters	1
Input Debouncing	Yes
Timestamp Generator	Yes
Timestamp Trigger	Yes
Software Controlled IO	4
GPIO Interrupts FIFO	Yes
Other	
Serial Ports (UART)	1 x LVTTL (Cam) 1 x LVTTL (Cam) (3.68) 1 x RS232 (GPIO) (Note 5)
Two-Wire Bus Interface 2	Optional (Note 4)
USRT	1 x LVTTL (Cam)
In-System JTAG	1 x LVTTL (Cam) (Note 5)
PT1000-VB Supply Voltage	Min: 4.5 V Typ: 5 V Max: 16 V
Power Consumption (measured at 10V)	Typ: 2.2 W Max: 2.4 W
Operating Temperature	Min: 0 °C Max: 70 °C
Storage Temperature	Min: -40 °C Max: 125 °C

Frame Grabber	
Ethernet Bandwidth	1 Gb/s
Unicast	Yes
Multicast	Yes
BOOTP	Yes
DHCP	Yes (4.06)
Number of Data Channels	1 (Std) Up to 4 (Opt)
Video Sources per Data Channel	1, 2, or 3 (4 Opt.) (Note 4)
Video Input	LVTTL, LVCMOS
Interlaced	Yes (SPARE used as FID)
Progressive Scan	Yes
Area Scan	Yes
Line Scan	Yes
Color	RGB, Bayer
Monochrome	Yes
PT1000-VB Data Output Formats	Grayscale Bayer RGB
Pixel Depth (bits)	8, 10, 12, 14, 16, 24, 32 (Opt)
Pixel Clock	Min: 1 MHz Max: 80 MHz
Taps per Data Channel	2 (Std) (Note 1) 4 (Opt)
Image Width (pixels) (must be multiple of 4)	Min: 4 Default: 640 Max: 16,380
Image Height (pixels)	Min: 1 Default: 480 Max: 16,383
Windowing	Yes
Decimation	Yes
Decimation by Block	Yes
Tap Reconstruction	Optional (Note 4)
Data Port Mapping	Yes
Pixel Shifting	Yes
Pixel Inversion	Yes
Recording	Yes

Notes:

(x.xx) - Available since firmware version x.xx

NA - Not applicable

* All features supported by iPORT S/W 2.2.0

1 - RGB supported as single-tap, 24 bits

2 - Compatible with I2C

4 - NRE or other charges may apply. Contact Pleora.

5 - Contact Pleora for availability

Table 1: iPORT PT1000-VB-CL Characteristics and Features

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3.0 Connectors

As shown in Figure 1, the iPORT PT1000-VB-CL board has three connectors:

- One RJ45 Ethernet connector, shown as J1;
- One power and IO connector, the 12-pin connector shown as J2; and
- One camera connector, the 80-pin connector shown as J3.

The Ethernet connector is a standard RJ-45 plug. The part number is XMultiple XRJV-S-01-8-8. More information about this connector can be obtained from www.xmultiple.com. The next sections of this document provide further details about the other two connectors.

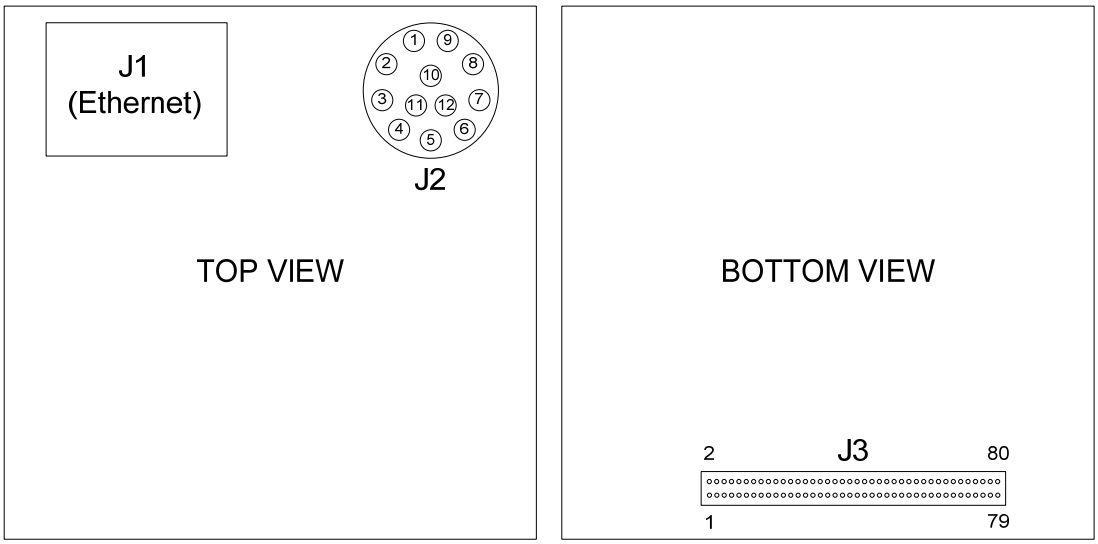

Figure 1: Connector Locations

3.1 Power and IO Connector

The power and IO connector (shown as J2 in Figure 1) is a Hirose HR10A-10R-12PB part. Note that this connector is not provided with the engine; only the mount for the connector is provided. More information about the connector can be obtained at www.hiroseusa.com. The mating part number is Hirose HR10A-10P-12S. Table 2 lists the 12 pins in the connector and describes the function of each.

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Pin	Signal Name	Type	Description
1	RET	PWR	Power return output
2	VIN	PWR	Power voltage input (5-15 V)
3	TTL_IN[3]	LVTTL	LVTTL input 3 (5 V tolerant)
4	TTL_OUT[2]	LVTTL	LVTTL output 2 (3.3 V output)
5	DGND	PWR	RMI Filtered Digital Ground (200 mA max.)
6	TTL_IN[2]	LVTTL	LVTTL input 2 (5 V tolerant)
7	TTL_OUT[1]	LVTTL	LVTTL output 1 (3.3 V output)
8	TTL_IN[1]	LVTTL	LVTTL input 1 (5 V tolerant)
9	TTL_OUT[0]	LVTTL	LVTTL output 0 (3.3 V output)
10	TTL_IN[0]	LVTTL	LVTTL input 0 (5 V compliant)
11	RS232_TX	RS232	RS232 transmit output[1]
12	RS232_RX	RS232	RS232 receive input[1]

Table 2: Power and IO Connector Pinout

3.2 Camera Connector

The camera connector (shown as J3 in Figure 1) is an 80-pin Samtec AW-40-03-G-D-230-075-A part. The mating part number is the 80-pin Samtec CLE-140-01-G-DV-A. Table 3 lists the 80 pins in the connector and describes the function of each. All signal levels are LVCMOS or LVTTL.

Pin	Signal Name	Type	Description
1	IN_CLK0	IN	Input Clock 0, Camera Link Input Clock (max 80 MHz)
2	OUT_CLK0	OUT	Output Clock 0, Configurable through FPGA PLL
3	DGND	PWR	Digital Ground
4	DGND	PWR	Digital Ground
5	PORT_A0	IN	DATA0, Camera Link Data Port A0
6	PORT_A1	IN	DATA1, Camera Link Data Port A1
7	PORT_A2	IN	DATA2, Camera Link Data Port A2
8	PORT_A3	IN	DATA3, Camera Link Data Port A3
9	PORT_A4	IN	DATA4, Camera Link Data Port A4
10	PORT_A5	IN	DATA5, Camera Link Data Port A5
11	PORT_A6	IN	DATA6, Camera Link Data Port A6
12	PORT_A7	IN	DATA7, Camera Link Data Port A7
13	PORT_B0	IN	DATA8, Camera Link Data Port B0
14	PORT_B1	IN	DATA9, Camera Link Data Port B1
15	PORT_B2	IN	DATA10, Camera Link Data Port B2
16	PORT_B3	IN	DATA11, Camera Link Data Port B3

[1] The RS232 interface is not currently implemented.

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Pin	Signal Name	Type	Description
17	DGND	PWR	Digital ground
18	DGND	PWR	Digital ground
19	PORT_B4	IN	DATA12, Camera Link Data Port B4
20	PORT_B5	IN	DATA13, Camera Link Data Port B5
21	PORT_B6	IN	DATA14, Camera Link Data Port B6
22	PORT_B7	IN	DATA15, Camera Link Data Port B7
23	PORT_C0	IN	DATA16, Camera Link Data Port C0
24	PORT_C1	IN	DATA17, Camera Link Data Port C1
25	PORT_C2	IN	DATA18, Camera Link Data Port C2
26	PORT_C3	IN	DATA19, Camera Link Data Port C3
27	PORT_C4	IN	DATA20, Camera Link Data Port C4
28	PORT_C5	IN	DATA21, Camera Link Data Port C5
29	PORT_C6	IN	DATA22, Camera Link Data Port C6
30	PORT_C7	IN	DATA23, Camera Link Data Port C7
31	DVCC	PWR	Digital supply, 3.3 V[2]
32	DVCC	PWR	Digital supply, 3.3 V[2]
33	PORT_D0	IN	CL_SPARE, Camera Link Spare
34	PORT_D1	IN	CL_LVAL, Camera Link Line Valid
35	PORT_D2	IN	CL_FVAL, Camera Link Frame Valid
36	PORT_D3	IN	CL_DVAL, Camera Link Data Valid
37	PORT_D4	OUT	CL_CC1, Camera Link Camera Control 1, connected to LUT output Q4
38	PORT_D5	OUT	CL_CC2, Camera Link Camera Control 2, connected to LUT output Q5
39	PORT_D6	OUT	CL_CC3, Camera Link Camera Control 3, connected to LUT output Q6
40	PORT_D7	OUT	CL_CC4, Camera Link Camera Control 4, connected to LUT output Q7
41	PORT_E0	N/C	Reserved
42	PORT_E1	N/C	Reserved
43	PORT_E2	N/C	Reserved
44	PORT_E3	N/C	Reserved
45	DGND	PWR	Digital ground
46	DGND	PWR	Digital ground
47	PORT_E4	N/C	Reserved
48	PORT_E5	N/C	Reserved
49	PORT_E6	N/C	Reserved
50	PORT_E7	N/C	Reserved

[2] If using these supplies, please contact Pleora during the specification stage of your design. Also, these DVCC supplies are not recommended for analog circuitry. Analog circuitry should be driven from a separate 3.3 V supply.

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Pin	Signal Name	Type	Description
51	PORT_F0	IN	CL_SERTFG, Camera Link Serial to Frame Grabber (PORT_SERIAL_0 in SDK)
52	PORT_F1	OUT	CL_SERTC, Camera Link Serial to Camera (PORT_SERIAL_0 in SDK)
53	PORT_F2	IN	RXD, USRT Receive Data
54	PORT_F3	OUT	TXD, USRT Transmit Data
55	PORT_F4	OUT	SCK, USRT Serial Clock (Max. 16.666 MHz)
56	PORT_F5	IN	UART_RX, Receive Data[3] (PORT_SERIAL_1 in SDK)
57	PORT_F6	OUT	UART_TX, Transmit Data[1] (PORT_SERIAL_1 in SDK)
58	PORT_F7/IN_CLK3	N/C	Reserved
59	DGND	PWR	Digital ground
60	DGND	PWR	Digital ground
61	IN_CLK1	IN	Input Clock 1 (for multi-input device, not used)
62	IN_CLK2	IN	Input Clock 2 (for multi-input device, not used)
63	PWR_ON_RST#	OC	Power On Reset, Open Collector, can be asserted low to reset the module
64	AGND	PWR	Analog ground
65	DVCC	PWR	Digital supply, 3.3 V[4]
66	ANALOG_VID	IN	Analog Video
67	TDI	OUT	In-system JTAG TDI[5]
68	FPGA_SEL	IN	FPGA load select (load 0 or load 1) – internal pull-up
69	VIN'	PWR	Power from Connector J2
70	VIN'	PWR	Power from Connector J2
71	VIN'	PWR	Power from Connector J2
72	VIN'	PWR	Power from Connector J2
73	RET'	PWR	Ground Return from Connector J2
74	RET'	PWR	Ground Return from Connector J2
75	RET'	PWR	Ground Return from Connector J2
76	RET'	PWR	Ground Return from Connector J2
78	TDO	IN	In-system JTAG TDO[3]
78	No Connect	N/C	System may fail if connected (test pin)
79	TMS	OUT	In-system JTAG TMS[3]
80	TCK	OUT	In-system JTAG TCK[3]

Table 3: Camera Connector Pinout

[3] The UART is implemented only in firmware Version 3.68 or higher.

[4] If using this supply, please contact Pleora during the specification stage of your design. Also, the DVCC supply is not recommended for analog circuitry. Analog circuitry should be driven from a separate 3.3 V supply.

[5] In-system JTAG is not currently implemented, but for future in-field updates pins TDI and TDO must be connected via a 0-ohm resistor or an in-system TAP controller. See Section 5.2 for more details.

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4.0 Signal Handling

The iPORT PT1000-VB-CL handles signals in much the same way as other iPORT IP engine models. There are a few minor differences, which are described in this section.

4.1 GPIO Control Block

The Programmable Logic Controller (PLC) in the iPORT PT1000-VB-CL routes signals through a sophisticated GPIO Control Block. Figure 2 shows the GPIO Control Block signals for the iPORT PT1000-VB-CL. For further details on how the engines handle IO signals, see the “User’s Manual, Shared Features of iPORT IP Engines.”

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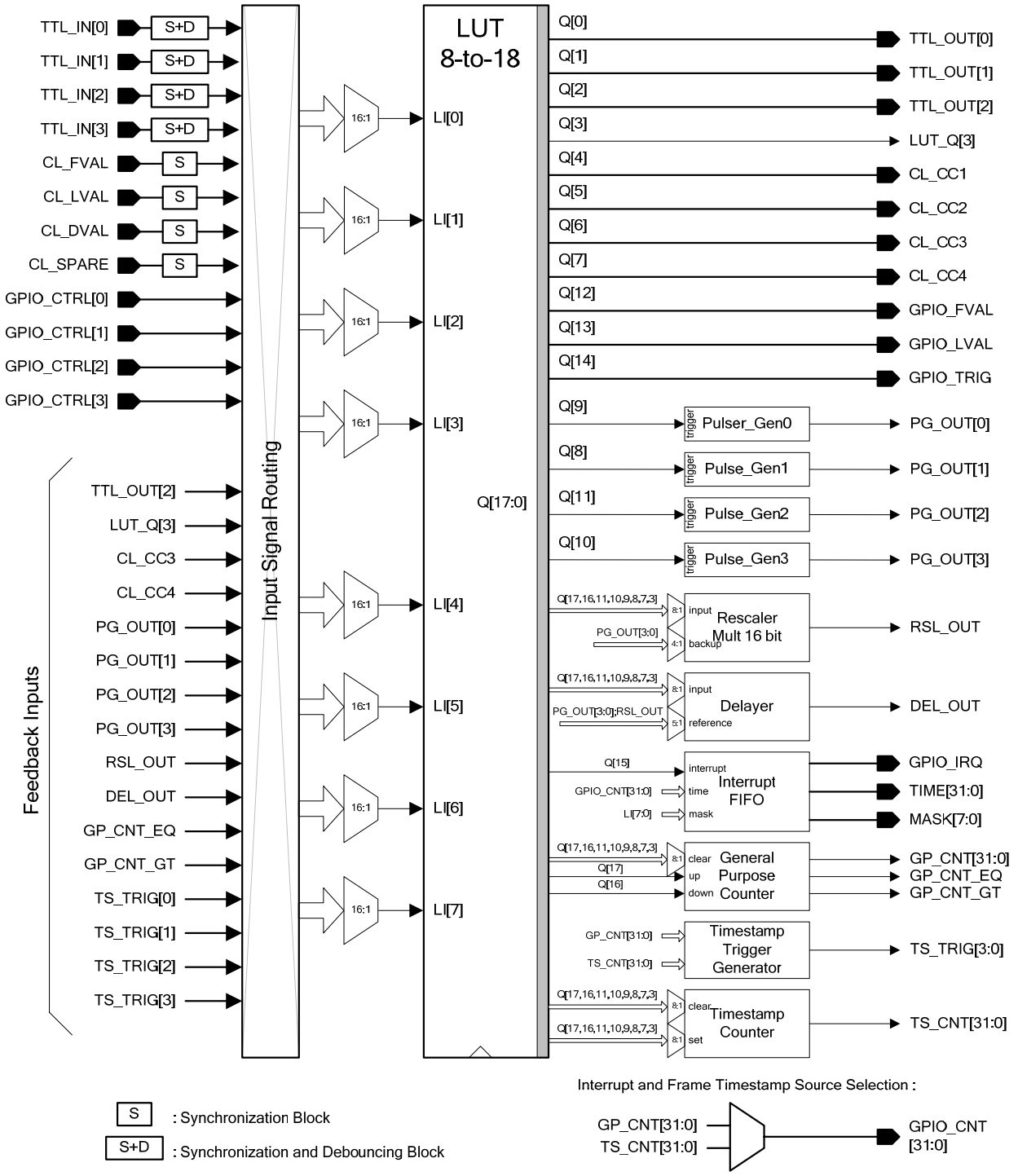

Figure 2: iPORT PT1000-VB-CL GPIO Control Block

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4.1.1 GPIO Programming Signals

Table 4 and Table 5 list the GPIO programming signals that are specific to the iPORT PT1000-VB-CL. The GPIO labels for inputs depend on the inputs configured in the GPIO Look-Up Table dialog. The GPIO labels for outputs are listed in the table.

Refer to "User's Manual, Shared Features of iPORT IP Engines" for details about other IO programming labels used by the engine.

Input Signal	Description
TTL_IN[0]	TTL Input 0
TTL_IN[1]	TTL Input 1
TTL_IN[2]	TTL Input 2
TTL_IN[3]	TTL Input 3
CL_FVAL	Camera Link Frame Valid signal
CL_LVAL	Camera Link Line Valid signal
CL_DVAL	Camera Link Data Valid signal
CL_SPARE	Camera Link Spare signal

Table 4: iPORT PT1000-VB-CL GPIO Input Signals

Output Signal	Label	Description
TTL_OUT[0]	Q0	Output 0
TTL_OUT[1]	Q1	Output 1
TTL_OUT[2]	Q2	Output 2
LUT_Q[3]	Q3	Feedback signal into GPIO Look-Up Table
CL_CC1	Q4	Camera Link control 1
CL_CC2	Q5	Camera Link control 2
CL_CC3	Q6	Camera Link control 3
CL_CC4	Q7	Camera Link control 4

Table 5: iPORT PT1000-VB-CL GPIO Output Signals

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4.2 Camera Interface

The iPORT PT1000-VB-CL provides a 28-bit, single-ended, LVTTL/LVCMOS, de-serialized, Camera Link compatible interface. This approach, which just removes the LVDS serializer, simplifies integration with existing Camera Link cameras. Please refer to the Camera Link specification for more details.

All Camera Link data and control signals are clocked by RXXCLK.[6]

See Section 4.2.4 for information about the Camera Link serial communications port.

4.2.1 Camera Inputs

All Camera Link camera heads have four standard signals: Camera Link Frame Valid (CL_FVAL), Camera Link Line Valid (CL_LVAL), Camera Link Data Valid (CL_DVAL), and Camera Link Spare (CL_SPARE). CL_FVAL and CL_LVAL can be activated by positive or negative signal edges, or by high or low levels. CL_DVAL can be activated by high or low levels.

The labels for these signals in the GPIO Control Block programming language depend on the inputs configured in the GPIO Look-Up Table dialog.

4.2.2 Camera Controls

The iPORT PT1000-VB-CL can send commands to the camera through the Camera Link Camera Control signals. The Camera Link specification provides four camera control signals, which can be used in a variety of ways.

The labels of the control outputs to the camera in the GPIO Control Block programming language are:

- Q4, for Camera Link CL_CC1
- Q5, for Camera Link CL_CC2
- Q6, for Camera Link CL_CC3
- Q7, for Camera Link CL_CC4

[6] This is the same signal as IN_CLK0 from Pin 1 in Table 3. Refer to Table 9 in Section 6.4.1 for the frequency specifications.

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4.2.3 Pixel Bus Definition

Table 6 lists all the configurations supported by the camera interface of the iPORT PT1000-VB-CL.

	CL Signal Name	Pixel Bus	8-bit	10-bit	12-bit	14-bit	16-bit	RGB
PORT_A0	RXXOUT[0]	DATA[0]	A0	A0	A0	A0	A0	R0
PORT_A1	RXXOUT[1]	DATA[1]	A1	A1	A1	A1	A1	R1
PORT_A2	RXXOUT[2]	DATA[2]	A2	A2	A2	A2	A2	R2
PORT_A3	RXXOUT[3]	DATA[3]	A3	A3	A3	A3	A3	R3
PORT_A4	RXXOUT[4]	DATA[4]	A4	A4	A4	A4	A4	R4
PORT_A5	RXXOUT[6]	DATA[5]	A5	A5	A5	A5	A5	R5
PORT_A6	RXXOUT[27]	DATA[6]	A6	A6	A6	A6	A6	R6
PORT_A7	RXXOUT[5]	DATA[7]	A7	A7	A7	A7	A7	R6
PORT_B0	RXXOUT[7]	DATA[8]	B0	A8	A8	A8	A8	G0
PORT_B1	RXXOUT[8]	DATA[9]	B1	A9	A9	A9	A9	G1
PORT_B2	RXXOUT[9]	DATA[10]	B2	N/C	A10	A10	A10	G2
PORT_B3	RXXOUT[12]	DATA[11]	B3	N/C	A11	A11	A11	G3
PORT_B4	RXXOUT[13]	DATA[12]	B4	B8	B8	A12	A12	G4
PORT_B5	RXXOUT[14]	DATA[13]	B5	B9	B9	A13	A13	G5
PORT_B6	RXXOUT[10]	DATA[14]	B6	N/C	B10	N/C	A14	G6
PORT_B7	RXXOUT[11]	DATA[15]	B7	N/C	B11	N/C	A15	G7
PORT_C0	RXXOUT[15]	DATA[16]	N/C	B0	B0	N/C	N/C	B0
PORT_C1	RXXOUT[18]	DATA[17]	N/C	B1	B1	N/C	N/C	B1
PORT_C2	RXXOUT[19]	DATA[18]	N/C	B2	B2	N/C	N/C	B2
PORT_C3	RXXOUT[20]	DATA[19]	N/C	B3	B3	N/C	N/C	B3
PORT_C4	RXXOUT[21]	DATA[20]	N/C	B4	B4	N/C	N/C	B4
PORT_C5	RXXOUT[22]	DATA[21]	N/C	B5	B5	N/C	N/C	B5
PORT_C6	RXXOUT[16]	DATA[22]	N/C	B6	B6	N/C	N/C	B6
PORT_C7	RXXOUT[17]	DATA[23]	N/C	B7	B7	N/C	N/C	B7

Table 6: Grabber Interface Pixel Bus Definition for the iPORT PT1000-VB-CL

The grabber input should be configured to match the camera head pixel bus, using the CY_GRABBER_PARAM_PIXEL_DEPTH and CY_GRABBER_PARAM_TAP_QUANTITY parameters of the CyGrabber class in the iPORT SDK. For the RGB configuration, the grabber should be set to 1 tap and 24 bits.

The grabber output can reformat the data using the CY_GRABBER_PARAM_NORMALIZED and CY_GRABBER_PARAM_PACKED parameters of the CyGrabber class. The structure

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of the resulting buffer is described in the Derived Pixel Type Classes of the Imaging Library section of the "Reference Manual, iPORT C++ Software Development Kit." The SDK also provides functions to swap input ports and to optimize bandwidth usage by shifting the input data.

4.2.4 Serial Interfaces

The PT1000-VB-CL has four serial interfaces that can send and receive data, as shown in Table 7.

Interface Type	Level	Port Name	Receive	Transmit	Clock
UART	LVCMOS/ LVTTL	Serial Port 0	CL_SERTFG (J3, pin 51)	CL_SERTC (J3, pin 52)	-
UART	LVCMOS/ LVTTL	Serial Port 1	UART_RX (J3, pin 56)	UART_TX (J3, pin 57)	-
USRT	LVCMOS/ LVTTL	Bulk Interface 0	RXD (J3, pin 53)	TXD (J3, pin 54)	SCK (J3, pin 55)
UART	RS232	TBA	RS232_RX (J2, pin 12)	RS232_TX (J2, pin 11)	-

Table 7: Serial Interfaces

Serial Port 0 and 1 are standard UARTs with selectable baud rates. For more information about these and the USRT interface, see Section 6.4.3 and 6.4.4 of this manual. In the future, users will be able to configure the Bulk Interface 0 port as a USRT, UART, or two-wire bus interface. At present, only the USRT interface is supported.

The RS232 interface is not currently implemented; contact Pleora if required. In the future, this interface will be able to bridge with one of the other serial interfaces. This will allow communication between the Hirose power and IO connector and the Samtec camera connector.

4.3 Passing Signals between the Hirose and Samtec Connectors

Upon request, Pleora can customize the PT1000-VB-CL to pass signals between the Hirose power and IO connector and Samtec camera connector. Through hardware modifications, one or both of the following configurations are offered:

J3, pin 64 (AGND) to J2, pin 3 (TTL_IN[3] disconnected)
J3, pin 66 (ANALOG_VID) to J2, pin 4 (TTL_OUT[2] disconnected)

Since these are direct short circuits between two pins, any type of signal level can be passed between them. As shown above, this modification can sacrifice one or both of the TTL_IN[3] and TTL_OUT[2] signals.

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5.0 Design Recommendations

This section presents some design recommendations and alternatives that should be considered in the initial stages of camera integration.

5.1 Power Supply Considerations

Power can be supplied to the PT1000-VB-CL from three different sources. Figure 3 illustrates how the different power supplies are related. There is one external (filtered) supply that is accessed via the Hirose power and IO connector (shown as J2). The other two supply sources are not filtered and are provided over the internal Samtec camera connector (shown as J3).

The only difference between the Hirose VIN/RET and the Samtec VIN'/RET' is a common-mode choke EMI filter (shown as L2) on the Hirose (external) versus the Samtec (internal) supplies. Otherwise either one, but not both, of the connectors can supply VIN/RET. DGND is a digital ground and not suitable for analog ground supplies due to switching noise. DGND must always be held at the same voltage level as RET (or RET').[7] DVCC has approximately 500 mA of available current at 3.3 V (1.65 W).

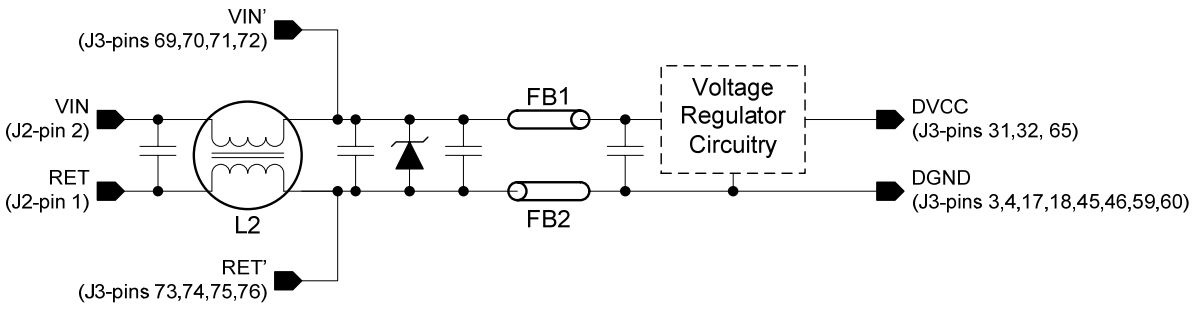

Figure 3: Simplified Schematic of the PT1000-VB-CL Power Supply Circuitry

[7] **CAUTION:** If there is a D.C. voltage difference between RET (or RET') and DGND it can damage the ferrite bead (FB2). The bead is rated up to only 2 A and has a DC resistance of only 50 mOhms. This damage can be caused by a simple misalignment of pins across the Samtec connector or when the Samtec connector is connected to a powered adapter.

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The three supply configurations are as follows:

1. Typical configuration - External VIN supply
   - Apply 5-15 V on VIN and ground RET on the Hirose (J2) connector
   - This supply is regulated and filtered
   - VIN'/RET' and DVCC/DGND can be used internally over the Samtec connector
   - Maximum current requirement (at 4.5 V) over the VIN/RET pins is 500 mA
2. Internal VIN Supply
   - Apply 5-15 V on VIN and ground RET on the Samtec (J3) connector
   - This supply is regulated and **not** filtered
   - DVCC/DGND can be used internally over the Samtec connector
   - VIN/RET can be used externally over the Hirose connector
   - Maximum current requirement (at 4.5 V) over the VIN'/RET' pins is 500 mA
3. Internal DVCC Supply
   - Apply 3.3 V to DVCC and ground GND on the Samtec (J3) connector.
   - DVCC must be generated by a fully regulated supply. This supply is not regulated or filtered on the PT1000-VB-CL

CAUTION: VIN and RET (or VIN' and RET') must be shorted together and connected to ground. Otherwise, the device may be damaged. Make sure that at least 2.25 W of power is available to this supply. The maximum current requirement (at 3.3 V) over the DVCC/DGND pins is 750 mA.

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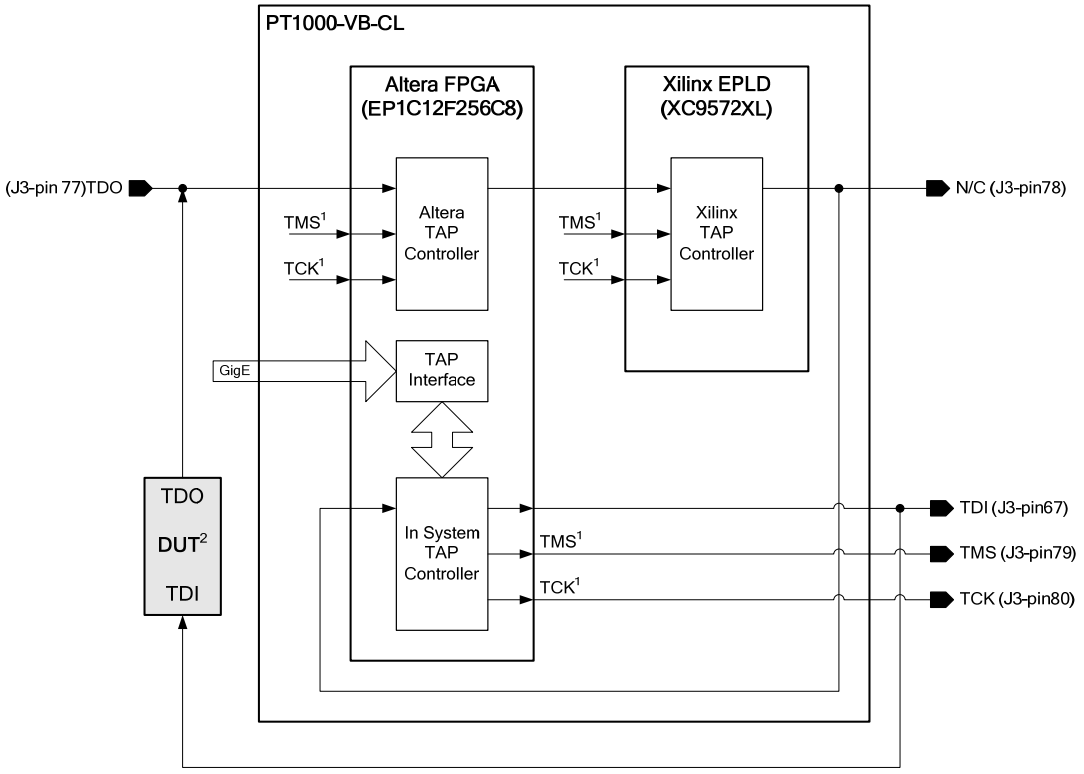
5.2 In-System JTAG

Figure 4 is a block diagram of the in-system JTAG architecture. To facilitate programming of the EPLD in the future, pins 67 and 77 of the 80-pin Samtec connector are connected together. If you want to use the in-system JTAG as well, then these pins should be coupled to the camera's TAP controller. This will allow field updates of any camera firmware over the GigE link. If pins 67 and 77 are not coupled using either of these methods, it will not be possible to update the EPLD or the camera in the field (via the GigE link).



(1) In Sytem, Altera and Xilinx JTAG share TMS and TCK
(2) It is highly recommended to couple pin 67 to pin 77 via an external TAP controller or, if the in-system JTAG controller is not required, via a zero Ohm resistor. If this is not done, certain upgrades cannot be performed in the field.

Figure 4: In-System JTAG Architecture

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5.3 FPGA_SEL Considerations

Figure 5 shows the FPGA_SEL options. The FPGA_SEL pin (J3, pin 68) is an input to the PT1000-VB-CL that selects a main (FPGA_SEL, high) or a back-up (FPGA_SEL, low) firmware load. Typically, this pin should not be driven. An internal pull-up resistor ensures that the main load is selected by default on power-up. In the unlikely event that the main load fails in the field and the engine cannot be updated remotely over the GigE link, then the back-up load can be selected.

It is therefore recommended that the FPGA_SEL pin be connected to a jumper so that it can be easily shorted to ground if a new main load must be programmed into memory, as shown in option (a) in Figure 5. It is also acceptable to just leave this pin unconnected, as shown in option (b). In the default configuration, it is critical to leave the pin in a high state.

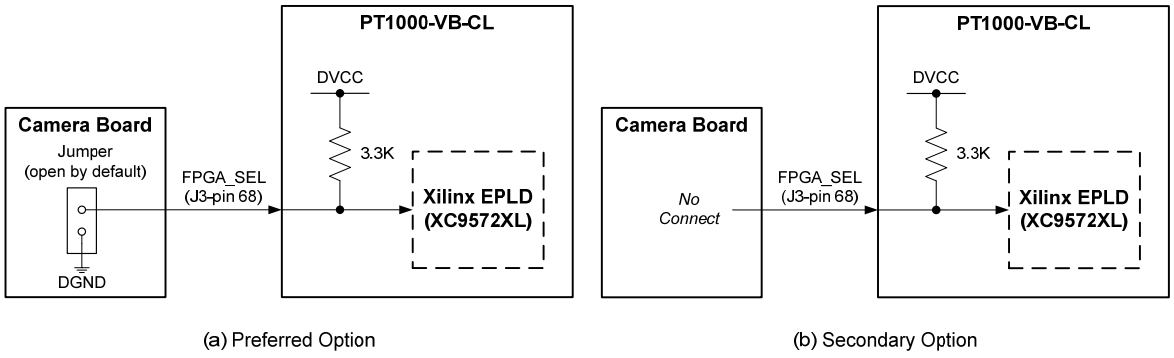

Figure 5: FPGA_SEL Options

5.4 EMI Considerations

In most cases, it is recommended to provide a good ground connection between the mounting screws and the enclosure. Please refer the “iPORT PT1000-VB In-Camera IP Engine: Design Recommendations for FCC/CE Certification” document for more details.

5.5 Unused Pins

All unused inputs in the Samtec (J3) and the Hirose (J2) connectors can be left floating. They will be held in a known state by weak internal pull-ups or pull-downs. Any unused outputs should be left unconnected, including unused supply outputs.

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6.0 Operating Characteristics

6.1 Absolute Maximum Ratings[8]

Ambient storage temperature ……. –40 °C to 125 °C

Ambient operating temperature……..…….. 0 °C to 70 °C

Voltage with respect to DGND:

VIN ……...…… -0.5 V to 25 V

DVCC ……...…… -0.5 V to 4.6 V

RS232_RX……...……. -25 V to 25 V

TTL_IN[3:0] ……...…….. -0.5 V to 7 V

All other pins……...…… -0.5 V to DVCC + 0.5 V

6.2 Recommended Operating Conditions

Ambient operating temperature (commercial)……..…… 0°C to +70°C

Supply voltages:

DVCC ……..…….. 3.0 V to 3.6 V

VIN ……..……..… 4.5 V to 16 V

[8] Stresses above those listed under Absolute Maximum Ratings may permanently damage the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this manual is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect reliability.

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6.3 D.C. Operating Characteristics

Table 8 shows the D.C. operating characteristics of the iPORT PT1000-VB-CL.

Parameter	Symbol	Min	Max	Units	Notes
Power			2.25	W	
RS232_RX	V_{IH}	2		V	
	V_{IL}		0.8	V	
RS232_TX	V_{OH}	5		V	RS232_TX at RL=3kΩ to DGND, RS232_RX = DGND
	V_{OL}	-5		V	RS232_TX at RL=3kΩ to DGND, RS232_RX = DVCC
TTL_IN[3:0]	V_{IH}	0.7 × DVCC		V	
	V_{IL}		0.3 × DVCC	V	
TTL_OUT[2:0]	V_{OH}	DVCC – 0.1		V	I_{OH} = -50 µA
	V_{OL}		0.1	V	I_{OL} = 50 µA
All other inputs	V_{IH}	0.7 × DVCC		V	
	V_{IL}		0.3 × DVCC	V	
All other outputs	V_{OH}	DVCC – 0.2		V	I_{OH} = -100 µA
	V_{OL}		0.4	V	I_{OL} = 51.6 mA

Table 8: D.C. Operating Characteristics

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6.4 A.C. Operating Characteristics

6.4.1 Camera Interface

Table 9 shows the A.C. sub-clock delays of the Camera Link control signals in the PT1000-VB. RXXCLK refers to IN_CLK0 and RXXOUT[27:0] refers to all the inputs of the camera interface (DATA[23:0], CL_FVAL, CL_LVAL, CL_DVAL, and CL_SPARE). Figure 6 is a timing diagram for the sub-clock delays.

Parameter	Symbol	Min	Max	Units	Notes
RXXCLK high-level width	t_{CH}	TBD		ns	
RXXCLK low-level width	t_{CL}	TBD		ns	
RXXCLK frequency	f_{CP}		80	MHz	
RXXCLK clock period	t_{CP}	12.5		ns	
RXXOUT setup time	t_{DS}	2		ns	By design
RXXOUT hold time	t_{DH}	2		ns	By design
CL_CC pulse width	t_{CCP}	30		ns	Asynchronous

Table 9: A.C. Sub-Clock Delays on the Camera Interface

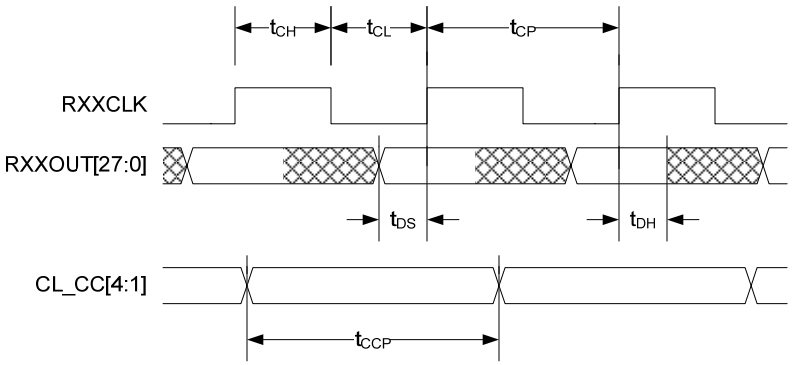

Figure 6: Timing Diagram of A.C. Sub-Clock Delays on the Camera Interface

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Table 10 shows the A.C. operating characteristics of the Camera Link control signals. Figure 7 to Figure 9 are the related timing diagrams.

Parameter	Symbol	Min	Max	Units	Notes
FVAL valid to LVAL valid	t_{FV2LV}				1
- FVAL and LVAL are level sensitive		0		t_{CP}	2
- FVAL is edge sensitive and LVAL is level sensitive		1		t_{CP}	
- FVAL and LVAL are edge sensitive		0		t_{CP}	3
FVAL valid to data valid	t_{FV2DV}				1, 4, 5
- FVAL and LVAL are level sensitive		0		t_{CP}	2
- FVAL is edge sensitive and LVAL is level sensitive		1		t_{CP}	
- FVAL and LVAL are edge sensitive		16		t_{CP}	3,7
LVAL valid to data valid	t_{LV2DV}				1, 4, 5
- LVAL is level sensitive		0		t_{CP}	
- LVAL is edge sensitive		1		t_{CP}	
LVAL valid to LVAL invalid	t_{LV2LI}	1		t_{CP}	1
LVAL invalid to LVAL valid	t_{LI2LV}	1		t_{CP}	1
LVAL invalid to data valid	t_{LI2DV}				1, 4, 5
- Automatic Internal Retrigger disabled		1		t_{CP}	
- Automatic Internal Retrigger enabled		16		t_{CP}	7
Data invalid to LVAL invalid	t_{DI2LI}				1, 4, 5
- LVAL is level sensitive		0		t_{CP}	
LVAL invalid to FVAL invalid	t_{LI2FI}				1
- FVAL and LVAL are level sensitive		0		t_{CP}	6
Data invalid to FVAL invalid	t_{DI2FI}				1, 4, 5
- FVAL and LVAL are level sensitive		0		t_{CP}	6
FVAL invalid to FVAL valid	t_{FI2FV}	1		t_{CP}	1
FVAL invalid to data valid	t_{FI2DV}	1		t_{CP}	1, 4, 5
Last LVAL invalid to data valid	t_{LLI2DV}	16			7
FVAL valid to invalid	t_{FV2FI}				
- FVAL is level sensitive		16		t_{CP}	7
- FVAL is edge sensitive		1		t_{CP}	
FVAL valid to valid	t_{FV2FV}	17		t_{CP}	7

Table 10: A.C. Operating Characteristics for Camera Link Signals

Notes:

(1) The valid state of FVAL and LVAL is high when they are set as level-high sensitive or rising-edge sensitive. Their valid state is low when they are set as level-low sensitive or falling-edge sensitive.

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(2) If LVAL is valid before FVAL becomes valid, then the full line is dropped by the grabber.

(3) The configuration FVAL as level-sensitive and LVAL as edge-sensitive is invalid and is seen as FVAL and LVAL edge-sensitive.

(4) Data valid is defined by FVAL valid (note 1), LVAL valid (note 1), and DVAL valid (note 5).

(5) The valid state of DVAL signal is high when it is set as level-high sensitive, and low when set as level-low sensitive. DVAL is always valid in the grabber when parameter DataValidEnabled is off.

(6) If FVAL becomes invalid and LVAL is still valid, the line is truncated.

(7) This is a worst case value. Three clock cycles can be subtracted if the pixel type is 8-bit, 1-tap, or 1 clock cycle for all other pixel types except 10/12-bit, 2-tap, unpacked and RGB unpacked. Up to seven clock cycles can be subtracted if the image size is a multiple of 32 bytes.

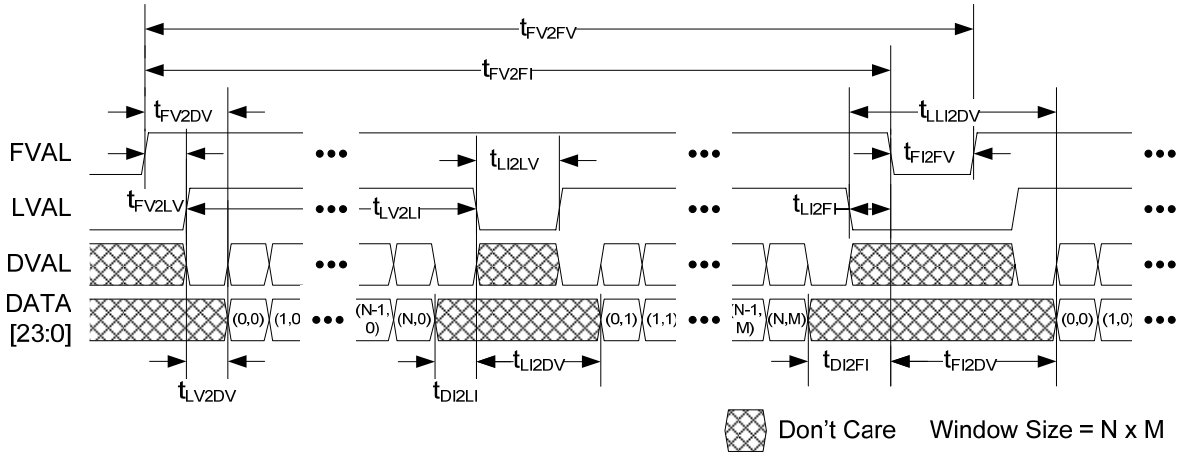

Figure 7: Camera Interface Timing When FVAL and LVAL are Level-Sensitive

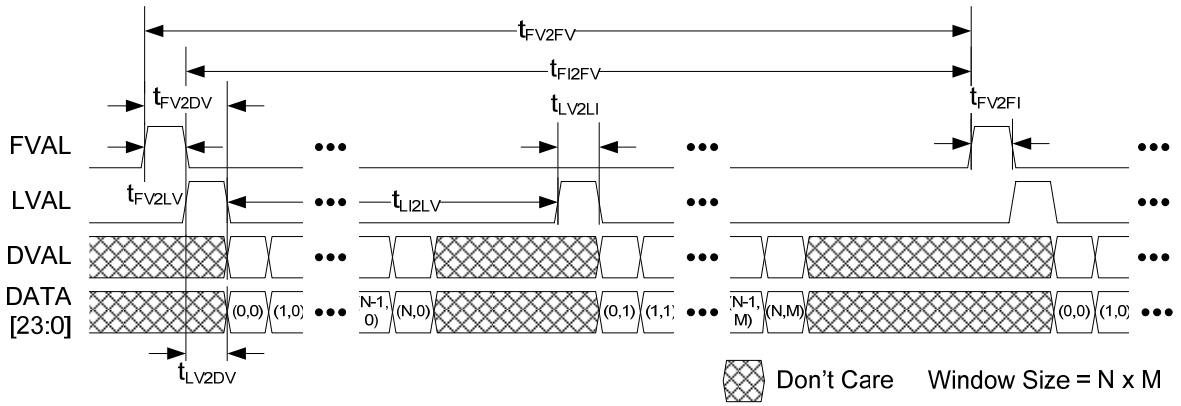

Figure 8: Camera Interface Timing with FVAL and LVAL Edge-Sensitive

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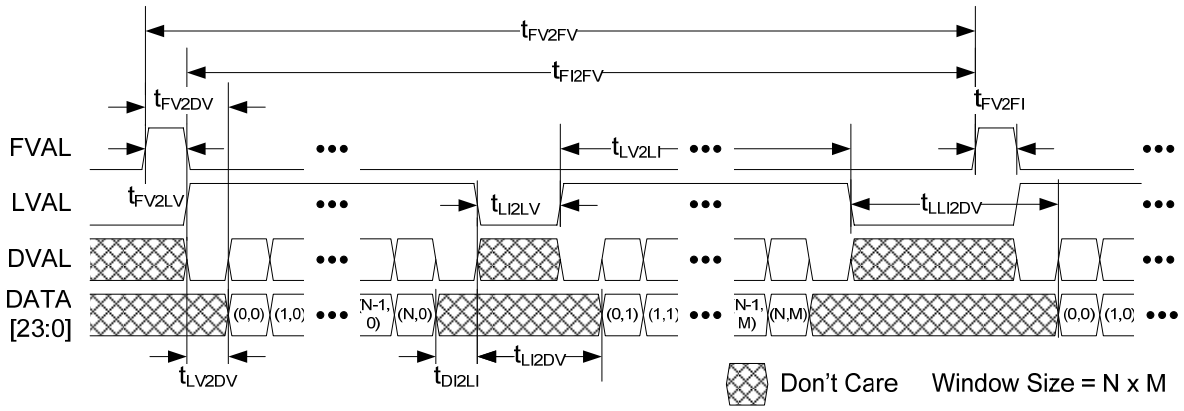

Figure 9: Camera Interface Timing with FVAL Edge-Sensitive and LVAL Level-Sensitive

6.4.2 GPIO Interface

The GPIO signals (TTL_IN[3-0] and TTL_OUT[2-0]) are all asynchronous and are specified below in Table 11. Figure 10 is the related timing diagram.

Parameter	Symbol	Min	Max	Units	Notes
GPIO Signal Pulse Width	t_{GPIOP}	30	-	ns	

Table 11: A.C. Operating Characteristics of the GPIO Signals

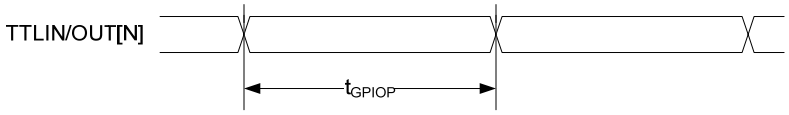

Figure 10: GPIO Timing Diagram

6.4.3 Serial Port (UART)

All three of the asynchronous serial ports/interfaces (CL_SERTFG/CL_SERTC, UART_RX/UART_TX and the RS232 interface) are UARTs. These interfaces only support 8-bit data transfer, 1 start bit, parity (even, odd, or none) and 1-2 stop bits. As shown in Table 12, a number of preset baud rates can be used, as well as a more flexible baud rate factor. See the "Reference Manual, iPORT C++ SDK" for more details.

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Baud Factor, BF	Baud Rate, BR [bps]	Notes
BF	1/(BF*480 ns)	Programmable
1 (min)	2,083,333	A baud factor of 0 is treated as a 1
18	115,200	Preset 6
36	57,600	Preset 5
54	38,400	Preset 4
72	28,800	Preset 3
109	19,200	Preset 2
145	14,400	Preset 1
217	9,600	Preset 0 (default)
255 (max)	8,170	

Table 12: UART Baud Rates

Parameter	Symbol	Min	Max	Units	Notes
Data Period	t_{UART}	0.480	122.4	µs	
Baud Rate	BR	8,170	2,083,333	bps	$1/T_{UART}$

Table 13: A.C. Operating Characteristics of the UART Interfaces

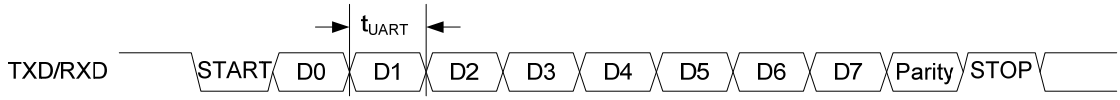

Figure 11: UART Timing Diagram

Table 13 shows the A.C. operating characteristics of the UART interfaces and Figure 11 is the related timing diagram. The UART only sends one byte at a time. The time between bytes is not deterministic and depends on the PC/host's available resources. This will slow down the effective baud rate such that the time to send 1 KB of data is the same for 9,600 baud and 115,200 baud. If a serial interface must move large amounts of data and/or transfer time is an issue, it is recommended that the bulk interface described in Section 6.4.4 be used.

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6.4.4 Bulk Interface (USRT and UART)

The bulk interface(s) can be configured as either USRT(s) or UART(s). These interfaces are intended for bulk data transfer. Please refer to the "Reference Manual, iPORT C++ SDK" for details on how to configure and use these ports. In particular, review the following functions:

- CyDevice::IsPortAvailable
- CyDevice::ConfigPort
- CyDevice::GetPortConfig
- CyDevice::GetPortConfigFormat
- CyDevice::SendCommand
- CyDevice::ReceiveAnswer
- CyDevice::ResetAnswerQueue
- CyDevice::GetAnswerQueueSize

6.4.4.1 UART Bulk Interface

This UART is specified in the same manner as the Serial Port. See Section 6.4.3 of this manual for more information. The main difference is that the delay between packets is significantly smaller and more predictable.

6.4.4.2 USRT Bulk Interface

Table 14 details the A.C. operating characteristics of the USRT and Figure 12 shows the timing of the related RXD/TXD and SCK signals.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Clock Period	T_{SCK}	60	-	960	ns	Programmable to 16.667, 8.333, 4.167, 2.083 and 1.041 MHz
SCK to TXD delay	t_{DTX}	-5	0	+5	ns	By design
RXD setup time	t_{SRX}	15			ns	By design
RXD hold time	t_{HRX}	0			ns	By design

Table 14: A.C. Operating Characteristics of the USRT Interface

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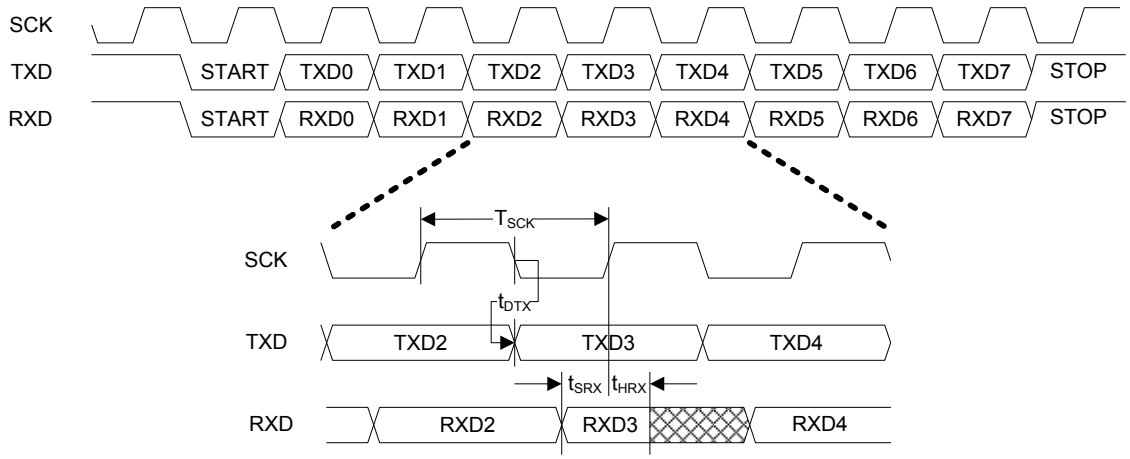

Figure 12: USRT Timing Diagrams

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7.0 Mechanical Dimensions

Figure 13 to Figure 16 are mechanical drawings of the iPORT PT1000-VB board (not to scale). The measurements are in inches unless otherwise specified, and have the following tolerances, depending on the number of significant digits provided:

.X	± 0.1
.XX	± 0.01
.XXX	± 0.005

The board is 0.0625 inches thick. The maximum secondary component height is 0.08 inches, unless otherwise specified.

Please note that the stacker height of the Samtec camera connector (referenced as HEADER 2x40 in Figure 16) is 0.230 inches high and its post height is 0.075 inches, for an overall pin height of 0.305 inches. Refer to the Samtec web site, www.samtec.com, for further details.

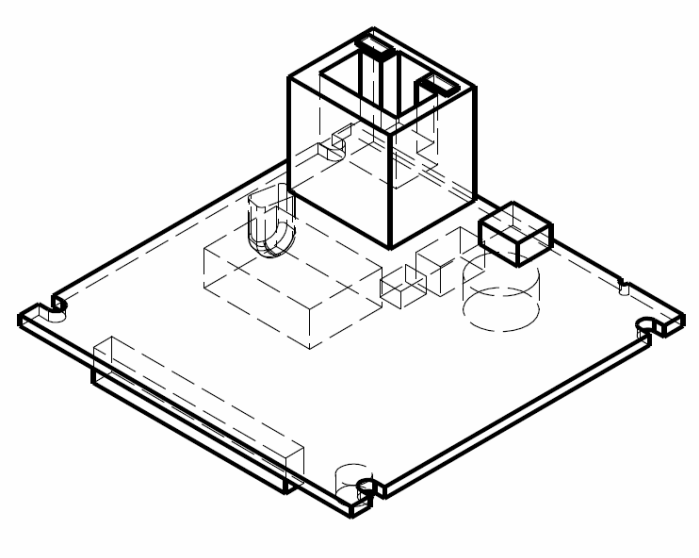

Figure 13: Isometric View

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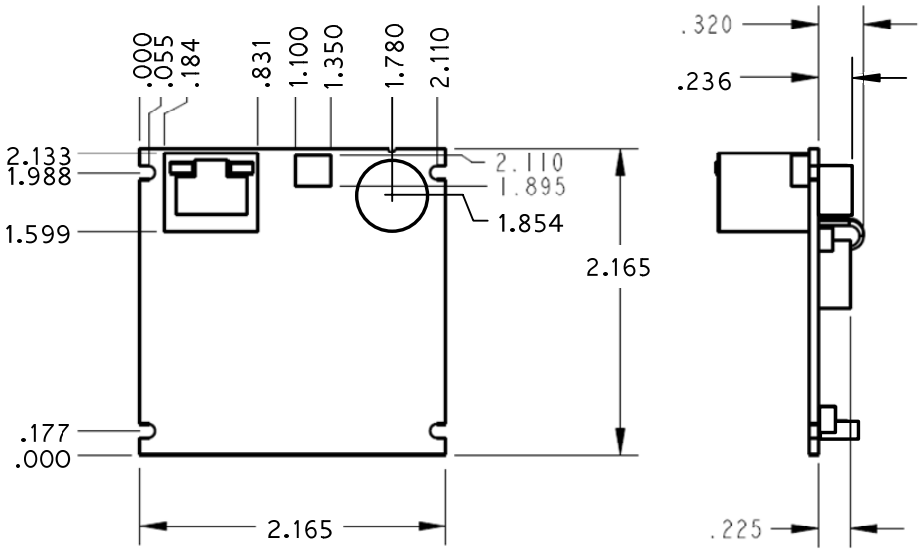
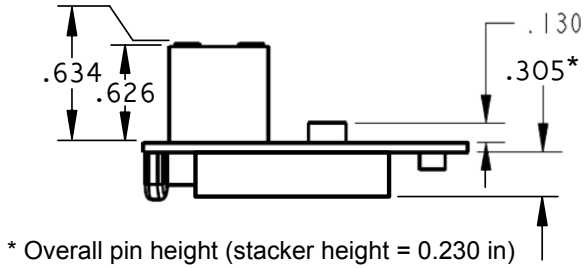


Figure 14: Top and Side View



* Overall pin height (stacker height = 0.230 in)

Figure 15: Front View

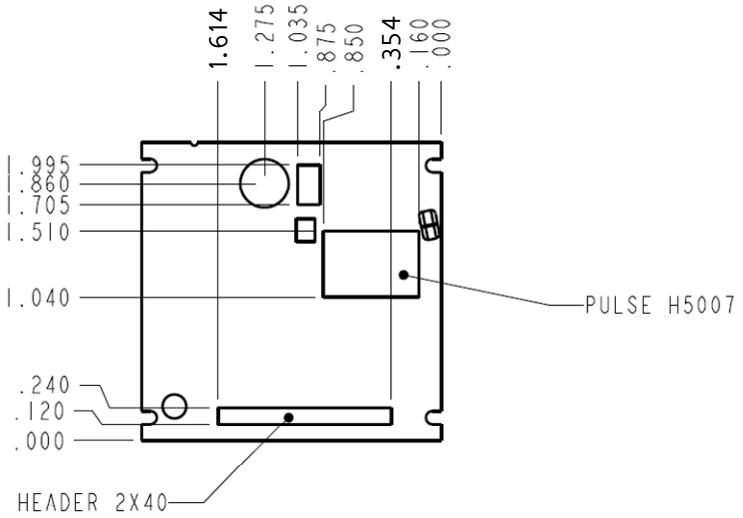


Figure 16: Bottom View

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8.0 Additional Support

Additional support can be obtained by contacting Applications Support at Pleora Technologies Inc. at (613) 270-0625 or via email at support@pleora.com.

8.1 Revision History

Revision	Date	Description
2.1.0	December 2004	Creation
2.1.1	June 2005	- Removed custom model - Added preliminary mechanical drawings - Updated connector location diagram - Added footnotes for the camera connector pinout in regards to the UART and In System JTAG - Updated the GPIO control block diagram
2.1.2	November 2005	- Updated mechanical drawings - Modified the tolerances - Added some connector information and links - Modified footnotes for the camera connector pinout table - Added new sections on serial interfaces, passing signals between connectors, design recommendations and operating characteristics - Modified the structure of the document
060206	February 2006	- Modified text to reflect iPORT Software V2.2.0 - Added Characteristics and Features table - Reordered sections - Updated formatting to comply with new Pleora template
060310	March 2006	- Updated Table 14

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